FIG. 1

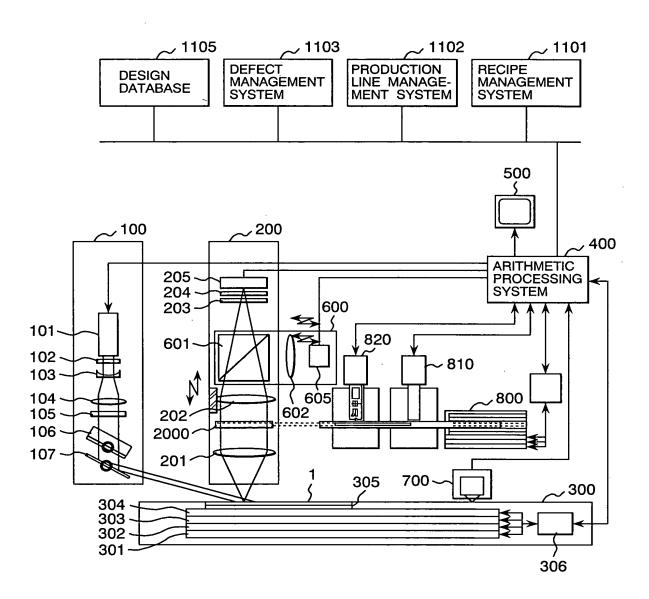


FIG. 2A

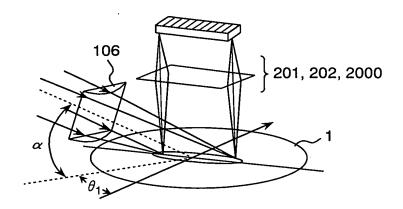


FIG. 2B

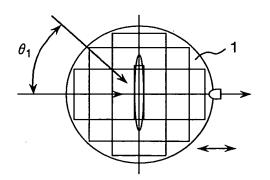


FIG. 3

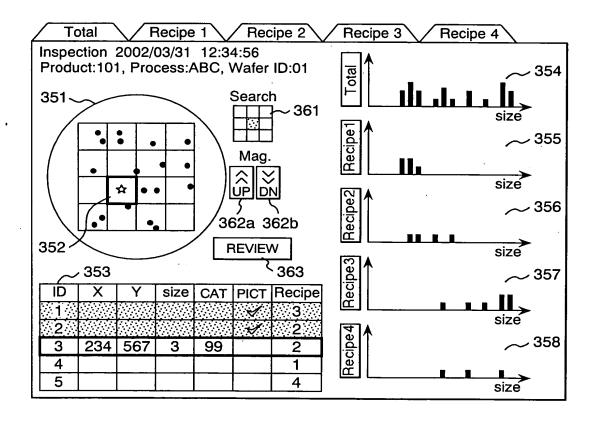


FIG. 4

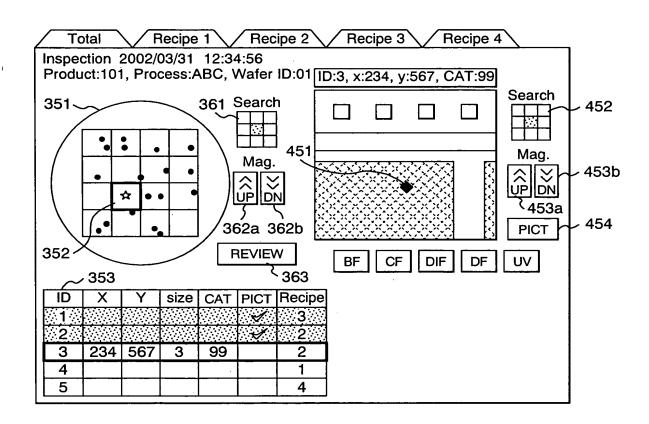


FIG. 5

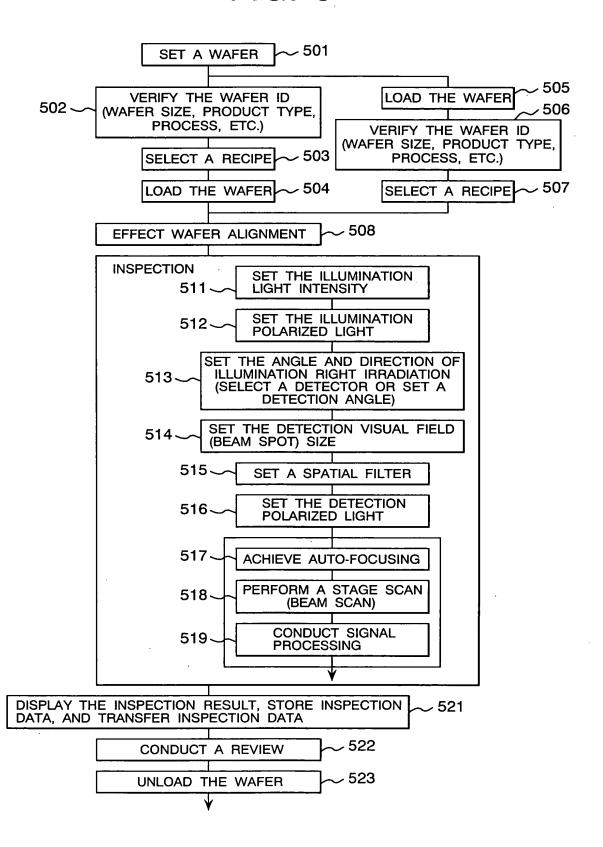
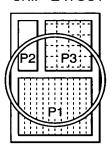


FIG. 6A

FIG. 6B

CHIP LAYOUT



PATTERN ON WAFER	P1	P2	P3
DIFFRAC- TED LIGHT PATTERN	FP1	FP2	FP3

FIG. 6C

OR OF FP1, FP2, AND FP3 OBSERVED FOURIER TRANSFORMED IMAGES



FIG. 7

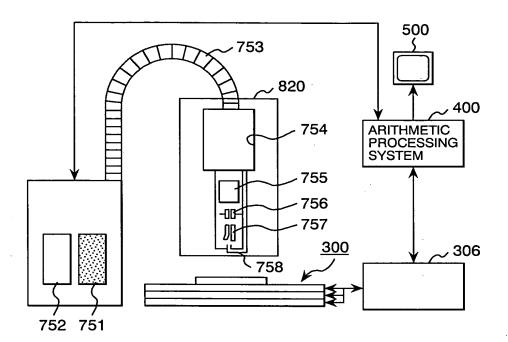
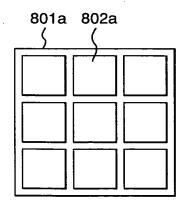


FIG. 8A

FIG. 8B



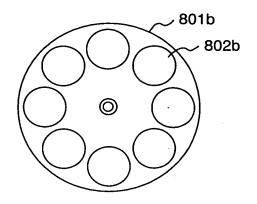


FIG. 9A

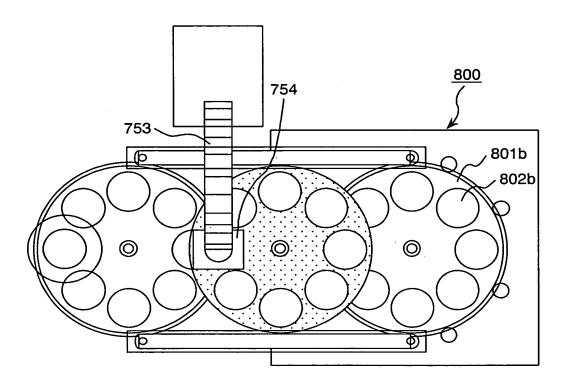


FIG. 9B

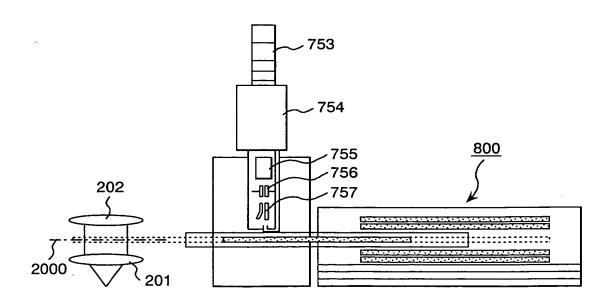


FIG. 10

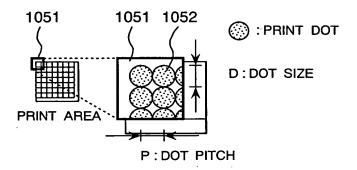
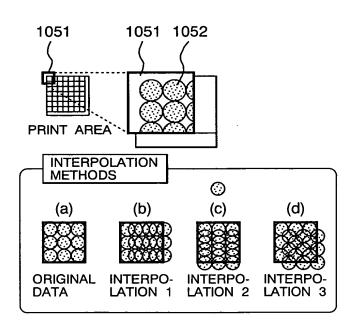


FIG. 11



## FIG. 12

## FOURIER TRANSFORM PLANE DIAMETER AND PRINT DOT SIZE

